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New U.S. Patent Application
Title: CIRCUIT DESIGNING APPARATUS, CIRCUIT DESIGNING METHOD, AND COMPUTER READABLE RECORDING MEDIUM STORING A CIRCUIT DESIGNING PROGRAM

Inventors: Takehiko Tsuchiya and Eiichi Yano

Sir:

We enclose the following papers for filing in the United States Patent and Trademark Office in connection with the above patent application.

1. A check for $ 886.00 representing a $ 846.00 filing fee and $ 40.00 for recording the Assignment.

2. Application - 20 pages, including 5 independent claims and 11 claims total.

3. Drawings - 5 sheets of formal drawings containing 7 figures.

4. Declaration and Power of Attorney.

5. Recordation Form Cover Sheet and Assignment to KABUSHIKI KAISHA TOSHIBA.

6. Information Disclosure Statement and Information Disclosure Citation, PTO 1449 with 3 documents attached.

Applicant claims the right to priority based on Japanese Patent Application No. P11-186819, filed June 30, 1999.

Please accord this application a serial number and filing date and record and return the Assignment to the undersigned.

The Commissioner is hereby authorized to charge any additional filing fees due and any other fees due under 37 C.F.R. § 1.16 or § 1.17 during the pendency of this application to our Deposit Account No. 06-0916.

Respectfully submitted,

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By: ______________________
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RVB/FPD/cb
Enclosures

CIRCUIT DESIGNING APPARATUS, CIRCUIT DESIGNING METHOD, AND COMPUTER READABLE RECORDING MEDIUM STORING A CIRCUIT DESIGNING PROGRAM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a circuit designing apparatus for feeding test vectors in the circuit description defining the structure and specification of the circuit to be designed, comparing the output signal and an expected value of output signal to verify the logic of the circuit description, and fabricating an actual circuit by using this circuit description, a circuit designing method, and a computer-readable recording medium storing a circuit designing program, and more particularly to a technique of shortening the time required for logic verification of circuit description so as to curtail the time and expense required for circuit design processing substantially.

2. Description of the Related Art

At the present, in a general circuit designing process, first, a circuit description defining the structure and specification of a circuit to be designed is prepared, and after judging the validity of the circuit description, a mask pattern is made from the circuit description, and an actual circuit is fabricated.

One of the techniques for judging the validity of the circuit description made in this circuit designing process is a process known as logic verification (for example, function verification, timing verification, and the like) for checking if the function of the circuit to be designed is realized according to the specification or not. In logic verification process, plural test vectors compiled by each function desired to be checked by the designer are fed into the circuit description, and the output signal and an expected value of output signal are compared. If the

output signal and its expected value are different, it is judged that the circuit description includes some inconvenience, and the defective position in the circuit description is corrected so as to realize a desired function.

However, this conventional logic verification process involves the following technical problems.

That is, usually, if any defect is detected in the circuit description by logic verification process, the defective position in the circuit description is corrected, but generally when the circuit description is changed, in order to check if a new unexpected bug (defective point) is mixed in by change, or check if the specification realized before is similarly realized after change, regardless of the content of change, it is necessary to process logic verification again by using all test vectors previously used in the logic verification process, and therefore in the conventional logic verification process, the time required for logic verification increases in proportion to the number of times of change of circuit description, possibly leading to a significant delay in the term of circuit designing process.

Besides, as the circuit to be designed is large in scale and complicated, the logic verification time required for one test vector is very long, and by the increase of the required verification items, the number of test vectors required for logic verification increases, and henceforth as the circuit becomes larger in scale and more complicated, such technical problems evidently become more and more serious.

SUMMARY OF THE INVENTION

The invention is devised in the light of the above technical problems, and it's object is to present a circuit designing apparatus capable of substantially curtailing the time required for circuit design.

Also, the other object of the invention is to present a circuit designing method capable of substantially curtailing the time required for circuit design.

And also, the further object of the invention is to present a computer-readable recording medium storing a circuit designing program capable of substantially curtailing the time required for circuit design.

To cope with these technical problems, the present inventors devised means for specifying the changed points of the circuit description automatically in predetermined unit, and classifying the plural test vectors into those related with the changed points and others not, and succeeded in curtailing the time required for circuit design substantially because the logic verification is done by using only the test vectors relating to the changed points in the second process of logic verification and after.

On the basis of this concept, a first feature of the present invention relates to a circuit designing apparatus comprising logic cone dividing unit for dividing a first circuit description defining the structure and specification of the circuit to be designed in logic cone units, logic verification unit for verifying the logic by using the first circuit description and test vectors, profile information generating unit for storing the information about the logic cone in the first circuit description to be activated by the test vector during logic verification in every test vector as profile information, circuit changing unit for changing the first circuit description and generating a second circuit description, formal verification unit for verifying by formal technology using the first and second circuit descriptions, logic cone specifying unit for specifying a changed logic cone relating to the change in the second circuit description on the basis of the result of formal verification, and test vector classifying unit for classifying the test vectors

into those activating the changed logic cone and others not by using the profile information.

A second feature of the present invention relates to a circuit designing method comprising a circuit description input step of entering a first circuit description defining the structure and specification of the circuit to be designed, a logic cone dividing step of dividing the first circuit description in logic cone units, a logic verification step of verifying the logic by using the first circuit description and test vectors, a profile information generating step of storing the information about the logic cone in the first circuit description to be activated by the test vector during logic verification in every test vector as profile information, a circuit changing step of changing the first circuit description and generating a second circuit description, a formal verification step of verifying by formal technology using the first and second circuit descriptions, a logic cone specifying step of specifying a changed logic cone relating to the change in the second circuit description on the basis of the result of formal verification, and a test vector classifying step of classifying the test vectors into those activating the changed logic cone and others not by using the profile information.

A third feature of the present invention relates to a computer-readable recording medium storing a circuit designing program for causing the computer to execute the processes comprising logic cone dividing process for dividing a first circuit description defining the structure and specification of the circuit to be designed in logic cone units, logic verification process for verifying the logic by using the first circuit description and test vectors, profile information generating process for storing the information about the logic cone in the first circuit description to be activated by the test vector during logic verification in every test vector as profile information,

circuit changing process for changing the first circuit description and generating a second circuit description, formal verification process for verifying by formal technology using the first and second circuit descriptions, logic cone specifying process for specifying a changed logic cone relating to the change in the second circuit description on the basis of the result of formal verification, and test vector classifying process for classifying the test vectors into those activating the changed logic cone and others not by using the profile information.

Herein, as the computer-readable recording medium, preferably, semiconductor memory, magnetic disk, optical disk, magneto-optical disk, magnetic tape, digital video disk and others may be used.

Logic verification process of the second circuit description may be executed by using preferentially the test vector for activating the changed logic cone.

Logic verification includes various verifications of circuit description using test vectors, such as function verification and timing verification.

According to the circuit designing apparatus of the present invention, when the circuit description is changed in logic verification, changed points in the circuit description are automatically specified in logic cone units, and plural test vectors are classified into those relating to the changed points and others not, and in the second and subsequent logic verification processes, therefore, without using all test vectors, verification is possible by using only the test vectors relating to the changed points, so that the time required for circuit design may be curtailed substantially. If there are plural changed points, logic verification can be executed sequentially from the test vector having the strongest relation, and therefore if the change itself is defective, it can be detected earlier. Moreover, it is possible to analyze which part of the

circuit is activated by a test vector, in the logic cone unit, by every test vector, so that the test vectors can be managed and controlled strictly.

Also, according to the circuit designing method of the present invention, when the circuit description is changed in logic verification, changed points in the circuit description are automatically specified in logic cone units, and plural test vectors are classified into those relating to the changed points and others not, and in the second and subsequent logic verification processes, therefore, without using all test vectors, verification is possible by using only the test vectors relating to the changed points, so that the time required for circuit design may be curtailed substantially. If there are plural changed points, logic verification can be executed sequentially from the test vector having the strongest relation, and therefore if the change itself is defective, it can be detected earlier. Moreover, it is possible to analyze which part of the circuit is activated by a test vector, in the logic cone unit, by every test vector, so that the test vectors can be managed and controlled strictly.

And also, according to the computer-readable recording medium storing a circuit designing program of the present invention, when the circuit description is changed in logic verification, changed points in the circuit description are automatically specified in logic cone units, and plural test vectors are classified into those relating to the changed points and others not, and in the second and subsequent logic verification processes, therefore, without using all test vectors, verification is possible by using only the test vectors relating to the changed points, so that the time required for circuit design may be curtailed substantially. If there are plural changed points, logic verification can be executed sequentially from the test vector having the strongest relation, and therefore if the

change itself is defective, it can be detected earlier. Moreover, it is possible to analyze which part of the circuit is activated by a test vector, in the logic cone unit, by every test vector, so that the test vectors can be managed and controlled strictly.

Other and further objects and features of the present invention will become obvious upon understanding of the illustrative embodiments about to be described in connection with the accompanying drawings or will be indicated in the appended claims, and various advantages not refereed to herein will occur to one skilled in the art upon employing of the invention in practice.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a configuration of a circuit designing system in an embodiment of the present invention.

Fig. 2 is a flowchart showing a circuit designing method in an embodiment of the present invention.

Fig. 3 is a flowchart showing an outline of a circuit designing system in an embodiment of the present invention.

Fig. 4 is a diagram showing an experimental example for explaining the logic verification process by the circuit designing method of the present invention.

Fig. 5 is a diagram showing an experimental example for explaining the logic verification process by the circuit designing method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Various embodiments of the present invention will be described with reference to the accompanying drawings. It is to be noted that the same or similar reference numerals are applied to the same or similar parts and elements throughout the drawings, and the description of the same or similar parts and elements will be omitted or simplified.

Prior to explanation of embodiments of the invention,

the term "logic cone" used herein is briefly described below.

In the circuit designing apparatus, circuit designing method, and computer-readable recording medium storing a circuit designing program according to embodiments of the present invention, the prepared circuit description is divided into predetermined units called "logic cones", and the information about logic cones is intensively used in logic verification process. This logic cone has a same technical meaning as the logic cone obtained by general formal verification process, and in a conical region (see Fig. 4 and Fig. 5) defined in every register in the circuit description, information of input signal relating to output signal to outside of each register or circuit is described. Therefore, by utilizing the information relating to the logic cone, the information relating to input and output of signals, such as defects in input and output of signals, in all region of the circuit can be obtained.

Referring now to Fig. 1 to Fig. 4, the circuit designing apparatus, circuit designing method, and computer-readable recording medium storing a circuit designing program accruing to embodiments of the present invention are described in detail below.

(Circuit designing system)

First, referring to Fig. 1, the configuration of the circuit designing system in an embodiment of the present invention is described below.

A circuit designing system 100 in the embodiment of the present invention comprises a circuit designing apparatus 110 for verifying the logic of the entered circuit description and correcting defects in the circuit description, input unit 120 for entering various parameters relating to the circuit description and circuit designing apparatus 110, and output unit 121 for issuing the corrected circuit description and error display, more

specifically the circuit designing apparatus 110 includes logic cone dividing unit 111 for dividing a circuit description defining the structure and specification of the circuit to be designed entered from the input unit 120 in logic cone units, logic verification unit 117 for verifying the logic by using the circuit description and test vectors, profile information generating unit 112 for storing the information about the logic cone in the circuit description to be activated by the test vector used in logic verification during execution of logic verification in every test vector as profile information, circuit changing unit 113 for changing the entered circuit description, formal verification unit 118 for verifying by formal technology using the circuit description before and after change, logic cone specifying unit 114 for specifying a logic cone relating to the change in the changed circuit description on the basis of the result of formal verification (changed logic cone), test vector classifying unit 115 for classifying the test vectors into those activating the changed logic cone and others not, and memory unit 116 for storing the profile information and various data.

Herein, as the input unit, the keyboard, mouse, and other input devices may be used, and the information stored in a floppy disk or other memory medium may be read out in the circuit designing apparatus 110. As the output unit, it is preferred to use a display device such as display screen and a printing device such as printer. The memory unit includes semiconductor memory, magnetic disk, optical disk, magneto-optical disk, magnetic tape, digital video disk, and others. Herein, the "test vector activating the changed logic cone" may be interpreted as "test vector passing through the changed logic cone."

(Circuit designing method))

Referring next to Fig. 2, a circuit designing method

according to an embodiment of the present invention is explained.

When designing the circuit according to the circuit designing method in the embodiment of the present invention, following processing steps is executed.

1. A first circuit description defining the structure and specification of the circuit to be designed is entered (circuit description input step, S101).
2. The first circuit description is divided in logic cone units (logic cone dividing step, S102).
3. The composition of logic cone in the first circuit description is stored so that the input and output information may be stored in every logic cone in the first circuit description (logic cone information storing (I) step, S103).
4. The logic is verified by using all test vectors necessary for first circuit description and verification (logic verification step, S104).
5. Information relating to the logic cone in the circuit description activated by each test vector used in logic verification during execution of logic verification step S104 (for example, information about test vector and logic cone activated by test vector) is stored as profile information in each test vector (profile information generating step, S105).
6. As a result of verification, judging if the desired function is realized by the first circuit description or not (defect judging step, S106), and when realized, the process goes to circuit description output step (S112), and if not realized, to circuit change step (S107).
7. In order to realize the desired function, the first circuit description is changed, and a second circuit description is prepared (circuit change step, S107).
8. Verifying by formal technology using the first and second circuit descriptions (formal verification step,

S108).

9. On the basis of the result of formal verification, the logic cone relating to the change in the second circuit description (changed logic cone) is specified (logic cone specifying step, S109).

10. Composition of logic cone in the second circuit description is stored so that input and output information may be stored in every logic cone within the second circuit description (logic cone information storing (II) step, S110).

11. Using the information relating to the changed logic cone and profile information, the test vectors used at the logic verification step S104 are classified into those activating the changed logic cone region and others not (test vector classifying step, S111), and only those activating (activating vectors) or test vectors greater in the number of activating logic cones are entered by priority in the circuit description, and the process after logic verification step (S104) is executed again.

12. Finally, by output of circuit description, using the corresponding circuit description, the mask pattern design, and subsequent circuit design, and manufacturing process are executed (circuit description output step, S112).

Thus, in the circuit designing method according to the embodiment of the present invention, when the circuit description is changed in logic verification, changed points in the circuit description are automatically specified in logic cone units, and plural test vectors are classified into those relating to the changed points and others not, and in the second and subsequent logic verification processes, therefore, without using all test vectors, verification is possible by using only the test vectors relating to the changed points, so that the time required for circuit design may be curtailed substantially. If there are plural changed points, logic verification can

be executed sequentially from the test vector having the strongest relation, and therefore if the change itself is defective, it can be detected earlier. Moreover, it is possible to analyze which part of the circuit is activated by a test vector, in the logic cone unit, by every test vector, so that the test vectors can be managed and controlled strictly.

It must be noted that the logic verification process mentioned in the specification includes various verifications of circuit description using test vectors, such as function verification and timing verification.

The circuit designing system 100 in the embodiment of the invention has an outlook as shown, for example, in Fig. 3. That is, the circuit designing system 100 according to the embodiment of the present invention is composed by incorporating the elements of the circuit designing apparatus 110 within the computer system 10. The computer system 10 includes a floppy disk drive 11 and an optical disk drive 13. A floppy disk 12 is inserted into the floppy disk drive 11, and an optical disk 14 is inserted into the optical disk drive 13, and by specified reading operation, the circuit designing programs stored in these recording media can be installed in the computer system 10. By connecting a proper drive device to the computer system 10, for example, a circuit designing program can be also installed by using a ROM 15 playing the role of memory device, or a cartridge 16 playing the role of a magnetic tape device.

The circuit designing apparatus 110 according to the embodiment of the present invention may be also programmed and stored in a computer-readable recording medium. When executing the circuit designing program, this recording medium is read in the computer system, and the circuit designing program is stored in the recording unit such as memory in the computer system, and by executing the process in the circuit designing program, the circuit designing

apparatus and its method of the embodiment of the present invention can be realized on the computer system. Herein, the recording medium includes, for example, semiconductor memory, magnetic disk, optical disk, magneto-optical disk, magnetic tape, digital video disk, and others that can record programs and can be read by a computer.

Finally, for deepening the understanding about the logic verification process in the circuit designing method of the invention, referring to Fig. 4 and Fig. 5, an example of logic verification process by using the circuit designing method of the present invention is briefly explained below.

Suppose a first circuit description defining the structure and specification is prepared as shown in Fig. 4 (a).

In logic verification of the first circuit description by the circuit designing method of the present invention,

(1) First, all test vectors 1 to 3 necessary for logic verification of the first circuit description are entered, and the logic is verified.

(2) During logic verification, the information of each one of the test vectors 1 to 3 activating which logic cone in the first circuit description is stored as profile information. In this case, specifically, the information of the test vector 1 activating logic cones 17a, 17b, test vector 2 activating logic cones 17e, 17c, 17d, and test vector 3 activating logic cone 17f is stored in the profile information.

(3) Referring to the result of logic verification, the first circuit description is changed, and a second circuit description as shown in Fig. 4 (b) is prepared.

(4) Verifying by formal technology using the first and second circuit descriptions and it is specified which logic cone in the second circuit description has been changed.

In this example, the logic cone 17d is changed, and it is assumed to be a changed logic cone.

(5) Using the profile information, a vector for activating the changed logic cone 17d (activating vector) is specified from the test vectors 1 to 3. In this example, it is supposed that the test vector 2 activates the logic cone 17d.

(6) Only the test vector 2 is put in the circuit description, and a second logic verification is executed.

In this example, if a new defect is detected in the second circuit description, the second circuit description is regarded as the first circuit description, and the same process is executed again. In this case, therefore, verifying by using formal technology in the second circuit description and third circuit description, and as a result of formal verification, if it is found that the output of the logic cone 17c has been newly added to the input of the logic cone 17f, the test vectors activating the logic cones 17c and 17f are searched by using the profile information of the second circuit description (in this case, the stored information shows the test vector 1 activating logic cones 17a, 17b, test vector 2 activating logic cones 17e, 17c,17d, and test vector 3 activating logic cone 17f). As a result, it is found that the test vectors 2 and 3 are activating the logic cones 17c and 17f, and in this stage, using the test vectors 2 and 3 only, the logic is verified. When a new circuit occurs in the third circuit description, similarly, verifying by using formal technology in the third circuit description and fourth circuit description, and as a result of formal verification, if it is found that the logic cone 17d has been deleted, the test vector activating the logic cone 17d is searched by using the profile information of the third circuit description (in this case, the stored information shows the test vector 1 activating logic cones 17a, 17b, test vector 2 activating

logic cones 17e, 17c,17d, 17f and test vector 3 activating logic cone 17f). As a result, it is found that the test vector 2 is activating the logic cone 17d, and in this stage, using the test vector 2 only, the logic is verified.

OTHER EMBODIMENTS

Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without depending from the scope thereof.

Thus, the invention includes various embodiments not mentioned herein. Therefore, the technical scope of the invention is determined only by the following claims as rationally understood from the description above.

WHAT IS CLAIMED IS:

1. A circuit designing apparatus comprising:

unit for specifying the changed points of the circuit description automatically in predetermined unit, and classifying the plural test vectors into those related with the changed points and others not.

2. A circuit designing apparatus comprising:

dividing unit for dividing a first circuit description defining the structure and specification of the circuit to be designed in predetermined units;

logic verification unit for verifying the logic by using said first circuit description and test vectors;

profile information generating unit for storing the information about the predetermined unit in the first circuit description to be activated by the test vector during said logic verification in every test vector as profile information;

circuit changing unit for changing said first circuit description and generating a second circuit description;

formal verification unit for verifying by formal technology using said first and second circuit descriptions;

specifying unit for specifying the changed predetermined unit relating to the change in said second circuit description on the basis of the result of said formal verification; and

test vector classifying unit for classifying the test vectors into those activating the changed predetermined unit and others not by using said profile information.

3. A circuit designing method comprising the steps of:

specifying the changed points of the circuit description automatically in predetermined unit; and

classifying the plural test vectors into those

related with the changed points and others not,

wherein the second and subsequent logic verification processes are executed by using only the test vectors relating to the changed points.

4. A circuit designing method comprising the steps of:

entering a first circuit description defining the structure and specification of the circuit to be designed;

dividing said first circuit description in predetermined units;

verifying the logic by using said first circuit description and test vectors;

storing the information about the predetermined unit in said first circuit description to be activated by the test vector during logic verification in every test vector as profile information;

changing said first circuit description and generating a second circuit description;

verifying by formal technology using the first and second circuit descriptions;

specifying the changed predetermined unit relating to the change in said second circuit description on the basis of the result of said formal verification; and

classifying the test vectors into those activating the changed predetermined unit and others not by using said profile information.

5. The circuit designing method of claim 4, wherein the logic verification of the second circuit description is executed by using preferentially the test vector for activating the changed predetermined unit.

6. The circuit designing method of claim 4, further comprising the step of:

issuing a circuit description and processing circuit

manufacture by using said circuit description.

7. The circuit designing method of claim 5, further comprising the step of:

issuing a circuit description and processing circuit design and manufacture by using said circuit description.

8. A computer-readable recording medium storing a circuit designing program comprising and making the computer execute the processes of:

dividing process for dividing a first circuit description defining the structure and specification of the circuit to be designed in predetermined units;

logic verification process for verifying the logic by using the first circuit description and test vectors;

profile information generating process for storing the information about the predetermined unit in the first circuit description to be activated by the test vector during logic verification in every test vector as profile information;

circuit changing process for changing the first circuit description and generating a second circuit description, formal verification process for verifying by formal technology using the first and second circuit descriptions;

specifying process for specifying the changed predetermined unit relating to the change in the second circuit description on the basis of the result of formal verification; and

test vector classifying process for classifying the test vectors into those activating the changed predetermined unit and others not by using the profile information.

9. The computer-readable recording medium storing a circuit designing program of claim 8, wherein the logic

verification of the second circuit description is executed by using preferentially the test vector for activating the changed predetermined unit.

10. The computer-readable recording medium storing a circuit designing program of claim 8, comprising and making the computer execute the process of:

output process of a circuit description,

wherein circuit manufacture is processed by using said circuit description.

11. The computer-readable recording medium storing a circuit designing program of claim 9, further comprising and making the computer execute the process of:

output process of a circuit description,

wherein circuit manufacture is processed by using said circuit description.

ABSTRACT OF THE DISCLOSURE

A circuit designing apparatus comprising: unit for specifying the changed points of the circuit description automatically in predetermined unit, and classifying the plural test vectors into those related with the changed points and others not; wherein the second and subsequent logic verification processes are executed by using only the test vectors relating to the changed points. As a result, the time required for circuit design can be substantially curtailed.

FIG. 1

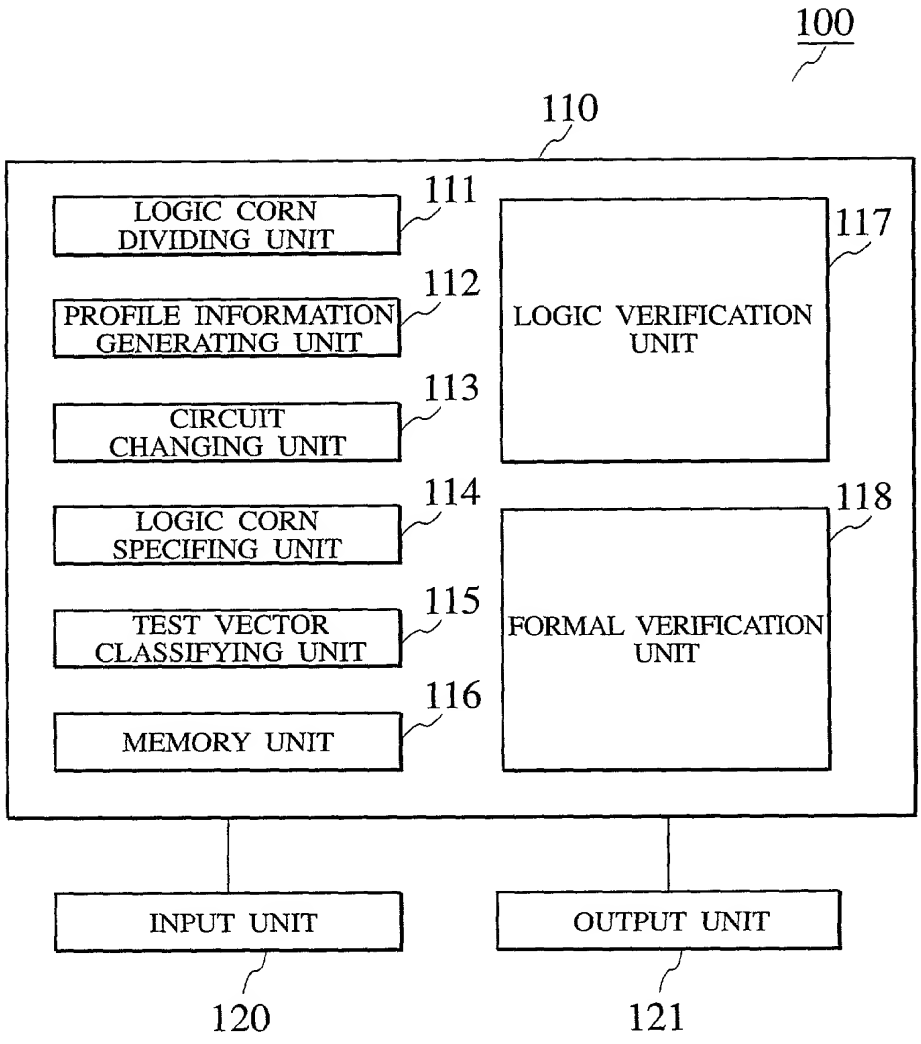


FIG. 2

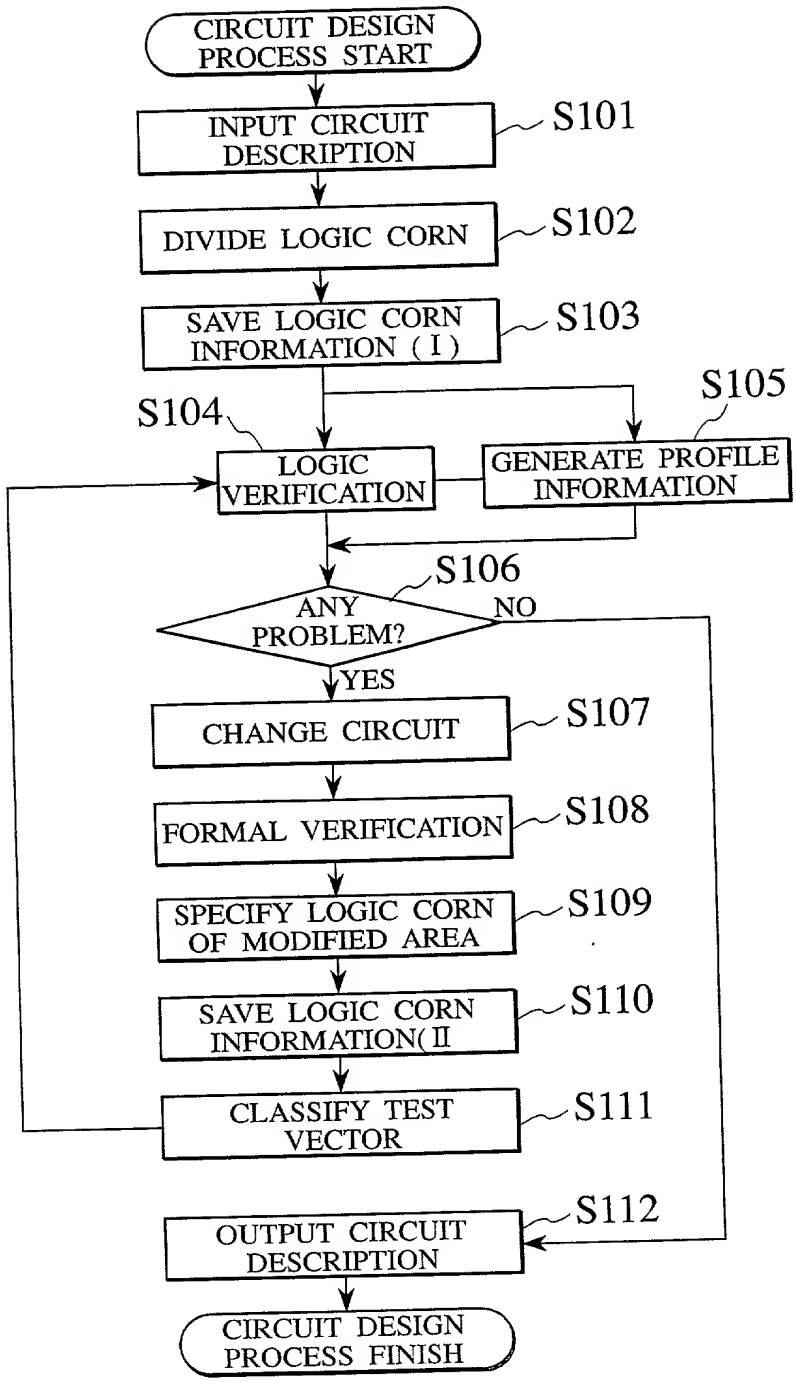

CIRCUIT DESIGN PROCESS START
INPUT CIRCUIT DESCRIPTION
S101
DIVIDE LOGIC CORN
S102
SAVE LOGIC CORN INFORMATION (I)
S103
S104
S105
LOGIC VERIFICATION
GENERATE PROFILE INFORMATION
S106
ANY PROBLEM?
NO
YES
CHANGE CIRCUIT
S107
FORMAL VERIFICATION
S108
SPECIFY LOGIC CORN OF MODIFIED AREA
S109
SAVE LOGIC CORN INFORMATION(II
S110
CLASSIFY TEST VECTOR
S111
OUTPUT CIRCUIT DESCRIPTION
S112
CIRCUIT DESIGN PROCESS FINISH

FIG. 3

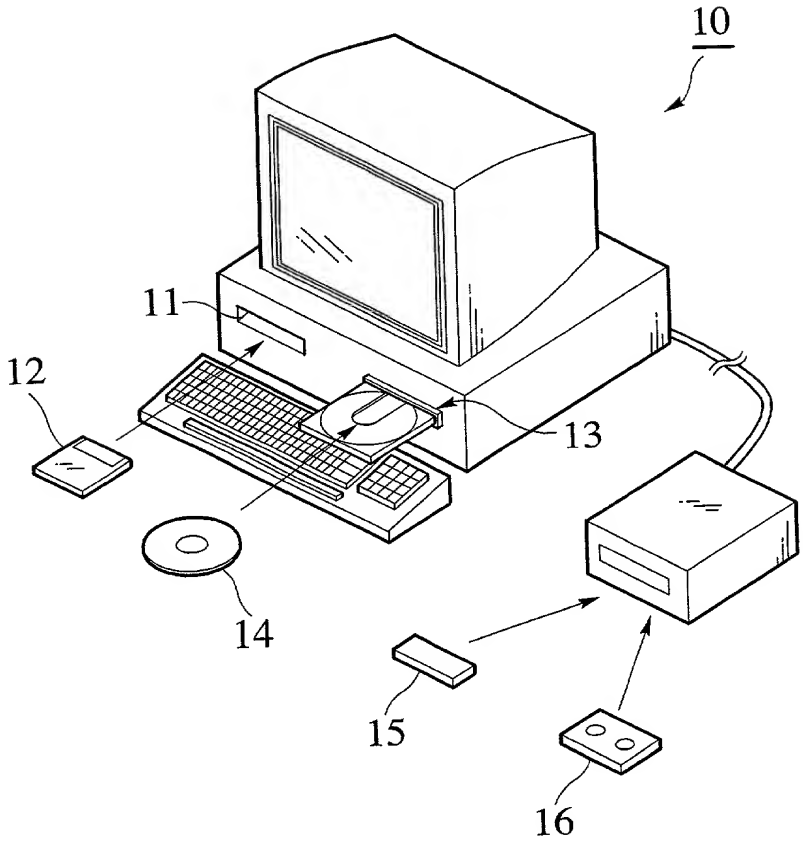


FIG. 4A

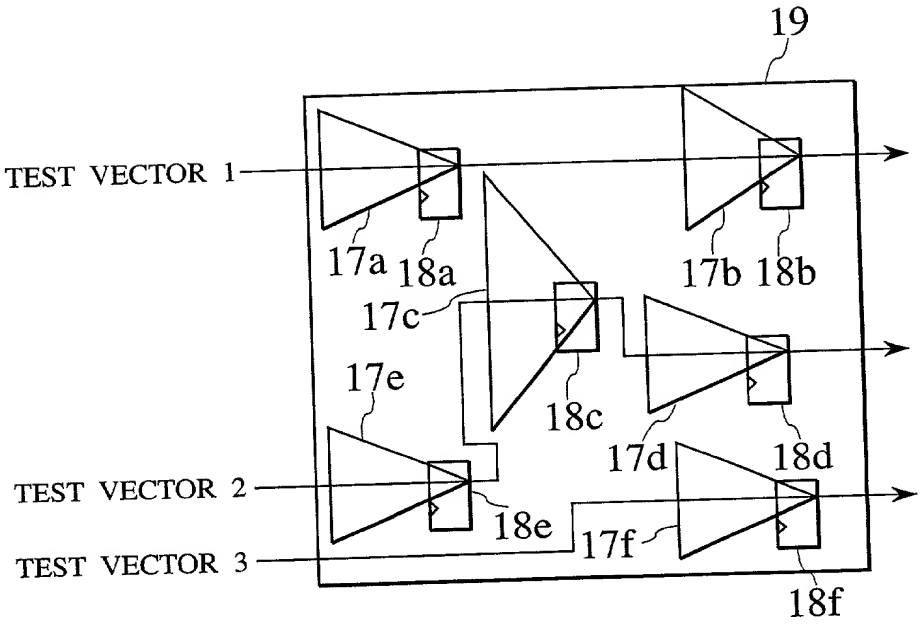
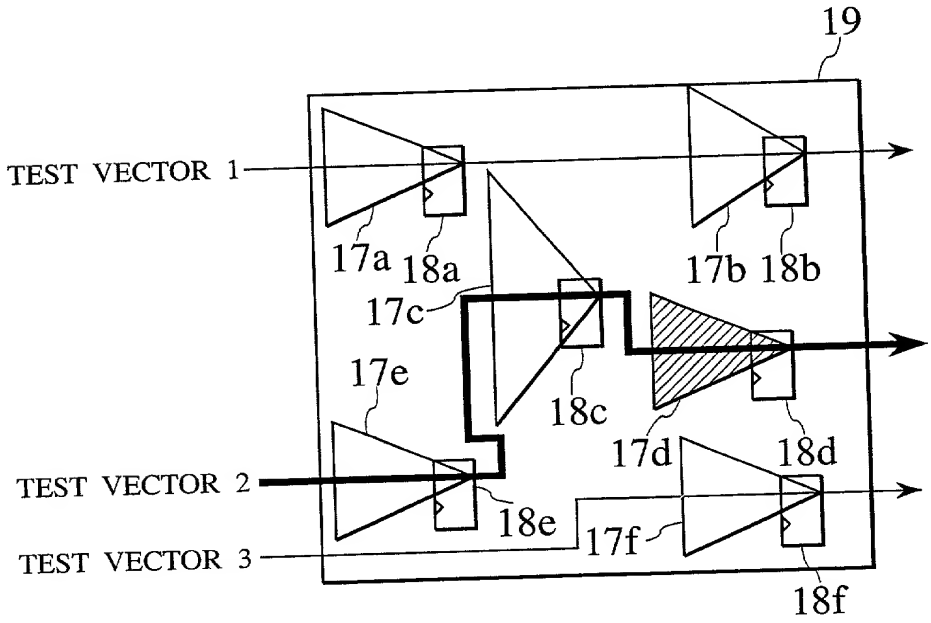


FIG. 4B



17a,b,c,d,e,f: LOGIC CORN
18a,b,c,d,e,f: REGISTER
19: INTEGRATED CIRCUIT

FIG. 5A

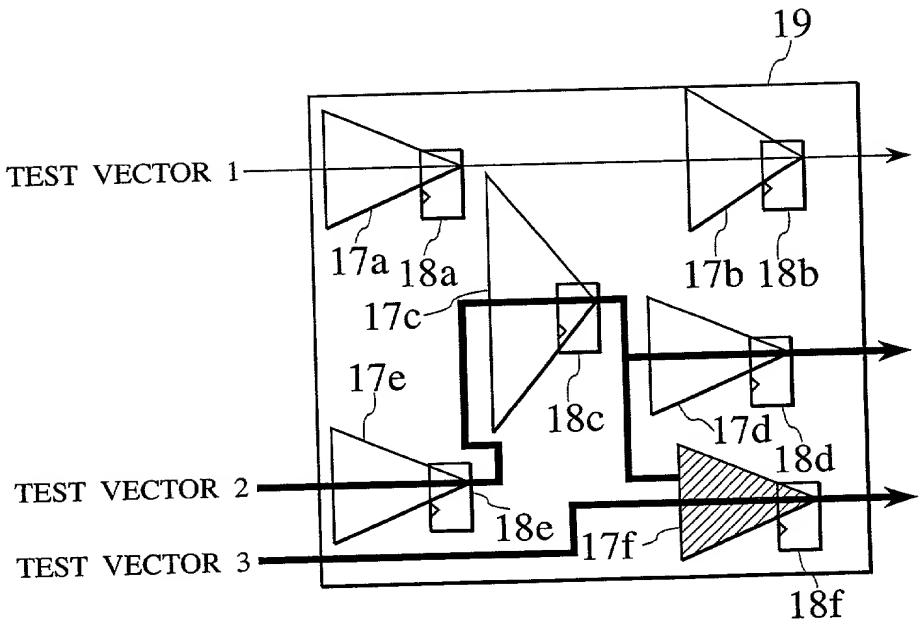
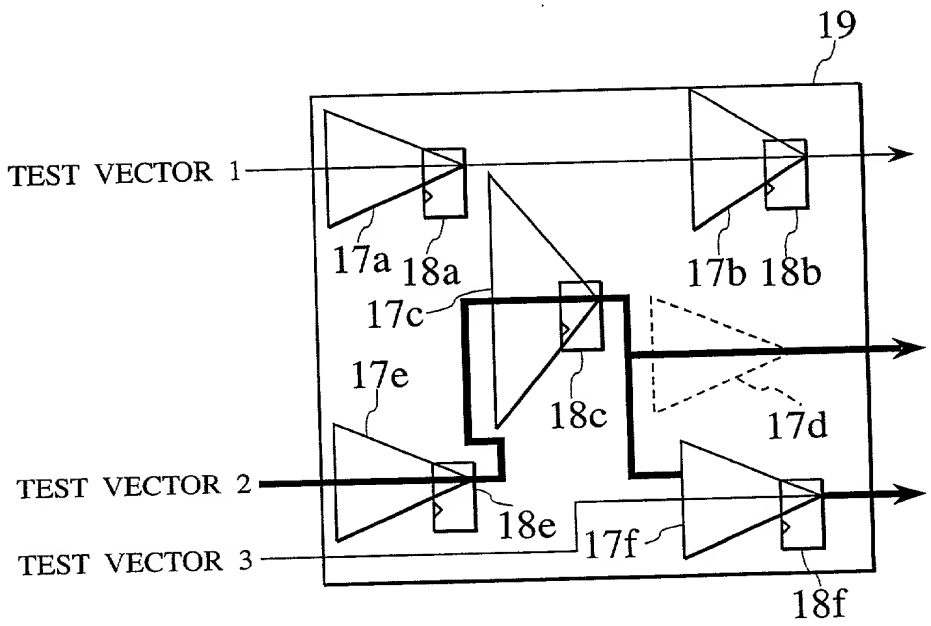


FIG. 5B



17a,b,c,d,e,f: LOGIC CORN
18a,b,c,d,e,f: REGISTER
19: INTEGRATED CIRCUIT

DECLARATION AND POWER OF ATTORNEY

Atty. Docket No.

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CIRCUIT DESIGNING APPARATUS, CIRCUIT DESIGNING METHOD, AND COMPUTER READABLE RECORDING MEDIUM STORING A CIRCUIT DESIGNING PROGRAM

the specification of which is attached hereto; or

was filed as United States application Serial No.
on and was amended
on _____ (if applicable); or

was filed as PCT international application Number
on and was amended
on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States, listed below and have also identified below, any foreign application(s) for patent or inventor's certificate, or any PCT international application(s) having a filing date before that of the application(s) of which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C.119
Japan	P11-186819	30/06/1999	X Yes ___ No
			___ Yes ___ No
			___ Yes ___ No
			___ Yes ___ No
			___ Yes ___ No
			___ Yes ___ No

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	DATE OF FILING

DECLARATION AND POWER OF ATTORNEY (Continued)

Atty. Docket No.

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) or § 365(c) of any PCT international application(s), designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application(s) in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

APPLICATIONS		STATUS (Check one)		
APPLICATION NUMBER	DATE OF FILING	PATENTED	PENDING	ABANDONED

I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. **FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P. Reg. No. 22,540;** Douglas B. Henderson, Reg. No. 20,291; Ford F. Farabow, Jr., Reg. No. 20,630; Arthur S. Garrett, Reg. No. 20,338; Donald R. Dunner, Reg. No. 19,073; Brian G. Brunsvold, Reg. No. 22,593; Tipton D. Jennings, IV, Reg. No. 20,645; Jerry D. Voight, Reg. No. 23,020; Laurence R. Hefter, Reg. No. 20,827; Kenneth E. Payne, Reg. No. 23,098; Herbert H. Mintz, Reg. No. 26,691; C. Larry O'Rourke, Reg. No. 26,014 Albert J. Santorelli, Reg. No. 22,610; Michael C. Elmer, Reg. No. 25,857; Richard H. Smith, Reg. No. 20,609; Stephen L. Peterson, Reg. No. 26,325; John M. Romary, Reg. No. 26,331; Bruce C. Zotter, Reg. No. 27,680; Dennis P. O'Reilley, Reg. No. 27,932; Allen M. Sokal, Reg. No. 26,695; Robert D. Bajefsky, Reg. No. 25,387; Richard L. Stroup, Reg. No. 28,478; David W. Hill, Reg. No. 28,220; Thomas L. Irving, Reg. No. 28,619; Charles E. Lipsey, Reg. No. 28,165; Thomas W. Winland, Reg. No. 27,605; Basil J. Lewris, Reg. No. 28,818; Martin I. Fuchs, Reg. No. 28,508; E. Robert Yoches, Reg. No. 30,120; Barry W. Graham, Reg. No. 29,924; Susan Haberman Griffen, Reg. No. 30,907; Richard B. Racine, Reg. No. 30,415; Thomas H. Jenkins, Reg. No. 30,857; Robert E. Converse, Jr., Reg. No. 27,432; Clair X. Mullen, Jr., Reg. No. 20,348; Christopher P. Foley, Reg. No. 31,354; John C. Paul, Reg. No. 30,413; David M. Kelly, Reg. No. 30,953; Kenneth J. Meyers, Reg. No. 25,146; Carol P. Einaudi, Reg. No. 32,220; Walter Y. Boyd, Jr., Reg. No. 31,738; Steven M. Anzalone, Reg. No. 32,095; Jean B. Fordis, Reg. No. 32,984; Barbara C. McCurdy, Reg. No. 32,120; James K. Hammond, Reg. No. 31,964; Richard V. Burgujian, Reg. No. 31,744; J. Michael Jakes, Reg. No. 32,824; Thomas W. Banks, Reg. No. 32,719; M. Paul Barker, Reg. No. 32,013; Bryan C. Diner, Reg. No. 32,409; Christopher P. Isaac, Reg. No. 32,616; Andrew Chanho Sonu, Reg. No.33,457; Dirk D. Thomas, Reg. No. 32,600; David S. Forman, Reg. No. 33,694; Vincent P. Kovalick, Reg. No. 32,867; James W. Edmondson, Reg. No. 33,871; Michael R. McGurk, Reg. No. 32,045; Joann M. Neth, Reg. No. 36,363; Gerson S. Panitch, Reg. No. 33,751; Cheri M. Taylor, Reg. No. 33,216; Charles E. Van Horn, Reg. No. 40,266; and _____.

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DECLARATION AND POWER OF ATTORNEY (Continued)

Atty. Docket No.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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